AN10933

2.5 GHz to 2.7 GHz Doherty power amplifier using the BLF7G27LS-150P

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Document information

Info	Content
Keywords	RF power transistor, Doherty architecture, LDMOS, RF performance, Digital PreDistortion (DPD), IS-95, W-CDMA, BLF7G27LS-150P
Abstract	This application note describes 2.5 GHz to 2.7 GHz RF performance tests for a Doherty power amplifier design using the BLF7G27LS-150P LDMOS power transistor

Revision history

Rev	Date	Description
01	20100816	Initial version

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1. Introduction

This application note describes RF performance tests over the range 2.5 GHz to 2.7 GHz for a Doherty power amplifier design using the BLF7G27LS-150P LDMOS power transistor.

The amplifier uses one BLF7G27LS-150P push-pull device in a Doherty architecture on a 0.76 mm (0.030") thick RF-35 printed-circuit board (PCB). One section functions as the main amplifier for the carrier signal, while the other functions as the peak amplifier for signal peaks. The design ensures high-efficiency while maintaining a very similar peak power capability of two sections of the push-pull device combined. The input and output sections are internally matched, contributing to high gain and good gain flatness and phase linearity over a wide frequency band.

The BLF7G27LS-150P is 150 W push-pull N-channel Enhancement-Mode Laterally Diffused MOSFET: a seventh generation LDMOS device using NXP Semiconductors' advanced LDMOS process.

The amplifier board layout is shown in Figure 1. The component layout is shown in Figure 12 on page 10and the list of components are given in Table 1 on page 11.

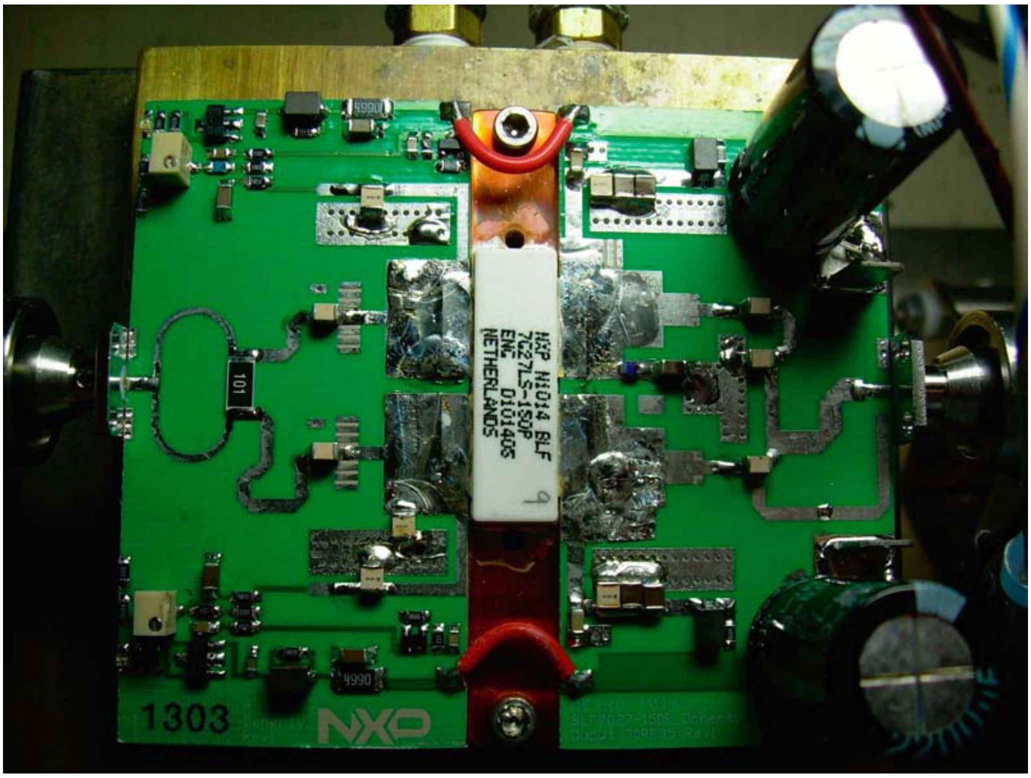

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Fig 1. BLF7G27LS-150P Doherty amplifier board layout

2. Test summary

Amplifier under test: board number: 1298; date code D101003BP.

The amplifier was set up and tested under the following conditions:

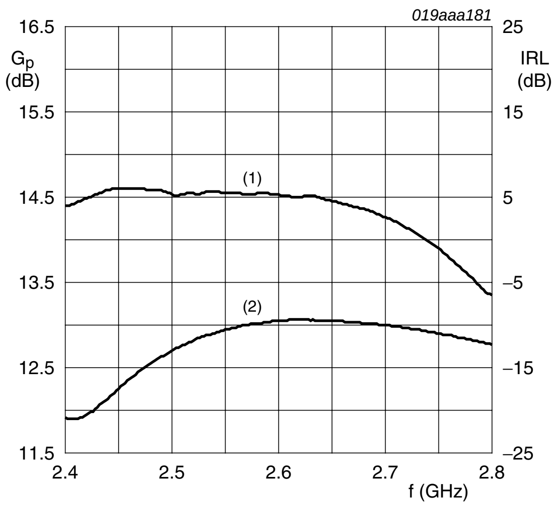
- Frequency band: 2500 MHz to 2700 MHz
- Network analyzer measurements for gain (G_p), delay (t_d) and Input Return Loss (IRL) at:
  - output power (P_L) = 43 dBm
  - drain-source voltage (V_{DS}) = 28 V
  - main power amplifier quiescent drain current ($I_{Dq\ (main)}$) = 500 mA
  - gate-source voltage of peak amplifier ($V_{GS\ (peak)}$) = 0.4 V
- CDMA Interim Standard (IS-95) at V_{DS} = 28 V, $I_{Dq\ (main)}$ = 500 mA and V_{GS} = 0.4 V
- Peak output power (P3dB) capability
  - using CDMA IS-95 signal, ratio of peak power to average power = 9.7 dB at 0.01 % probability, V_{DS} = 28 V, $I_{Dq\ (main)}$ = 500 mA and $V_{GS\ (peak)}$ = 0.4 V
  - using a pulsed signal and measuring the 3 dB compression points with a pulse width of 12 μs, 10 % duty cycle at V_{DS} = 28 V, $I_{Dq\ (main)}$ = 500 mA and $V_{GS\ (peak)}$ = 0.4 V
- Digital PreDistortion (DPD) measurements using a DPD system, 2-carrier W-CDMA signal, 10 MHz spacing, Peak-to-Average ratio (PAR) = 7.4 dB at 0.01 % probability (total signal), V_{DS} = 28 V, $I_{Dq\ (main)}$ = 500 mA, $V_{GS\ (peak)}$ = 0.4 V

3. RF Performance

3.1 Network analyzer measurements

Network analyzer measurements were made under the following conditions:

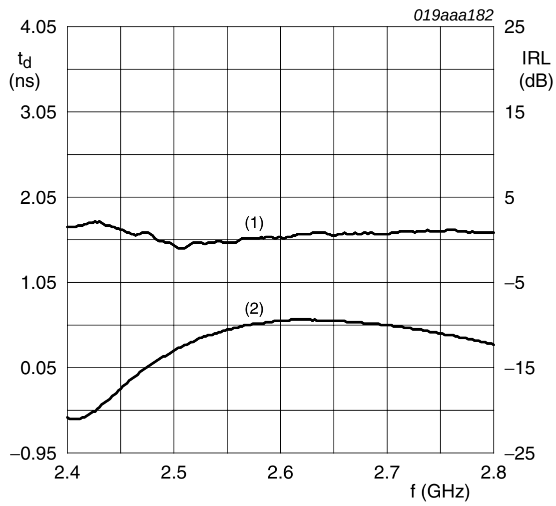
- P_L = 43 dBm
- V_{DS} = 28 V
- $I_{Dq\ (main)}$ = 500 mA
- $V_{GS\ (peak)}$ = 0.4 V



(1) G_p.

(2) IRL.

Fig 2. Power gain and input return loss as a function of frequency



(1) t_d.

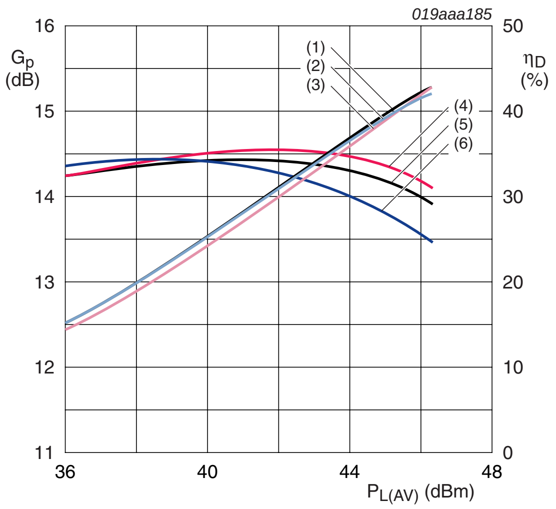
(2) IRL.

Fig 3. Delay and input return loss as a function of frequency

3.2 IS-95 measurements

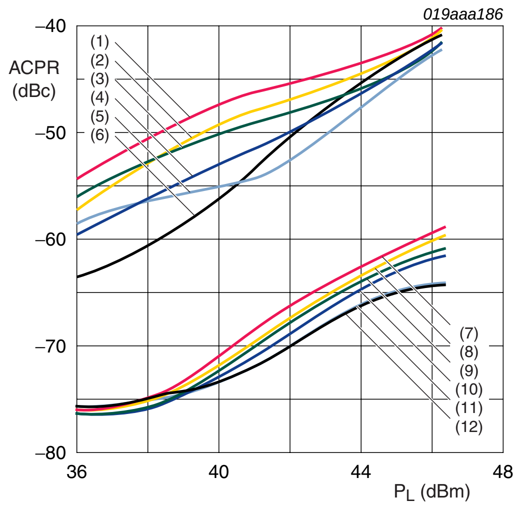
The IS-95 measurements were made under the following conditions:

- Bias: V_{DS} = 28 V
- $I_{Dq\,(main)}$ = 500 mA
- $V_{GS\,(peak)}$ = 0.4 V



(1) G_p = 2500 MHz.
(2) G_p = 2600 MHz.
(3) G_p = 2700 MHz.
(4) η_D = 2500 MHz.
(5) η_D = 2600 MHz.
(6) η_D = 2700 MHz.

Fig 4. Power gain and drain efficiency as a function of average output power, IS-95



(1) 2500 MHz − 885 kHz.
(2) 2500 MHz + 885 kHz.
(3) 2600 MHz − 885 kHz.
(4) 2600 MHz + 885 kHz.
(5) 2700 MHz − 885 kHz.
(6) 2700 MHz + 885 kHz.
(7) 2500 MHz − 1.98 MHz.
(8) 2500 MHz + 1.98 MHz.
(9) 2600 MHz − 1.98 MHz.
(10) 2600 MHz + 1.98 MHz.
(11) 2700 MHz − 1.98 MHz.
(12) 2700 MHz + 1.98 MHz.

Fig 5. Adjacent channel power ratio as a function of output power

3.3 Peak output power measurements

Two methods were used to measure peak output power.

- Using a standard IS-95 signal (PAR = 9.7 dB at 0.01 % probability on the CCDF), determining the output power where the PAR reaches 6.7 dB at 0.01 % probability on the CCDF, measured as the 3 dB compression point (Figure 6)
- Using the pulsed signal (12 μs width and 10 % duty cycle), measuring the 1 dB and 3 dB compression points (Figure 7)

The peak power measurements were made under the following conditions:

- Bias: V_{DS} = 28 V
- $I_{Dq\ (main)}$ = 500 mA
- $V_{GS\ (peak)}$ = 0.4 V

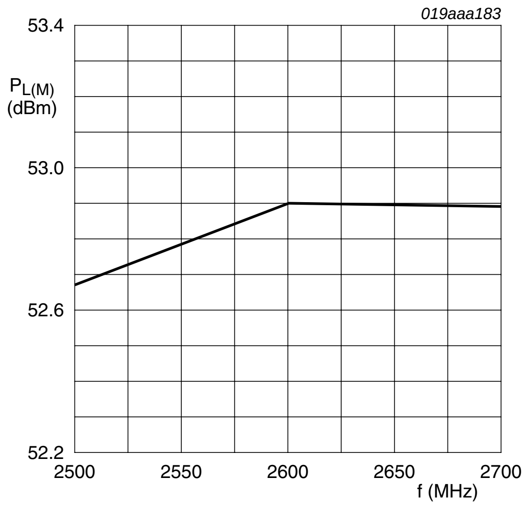
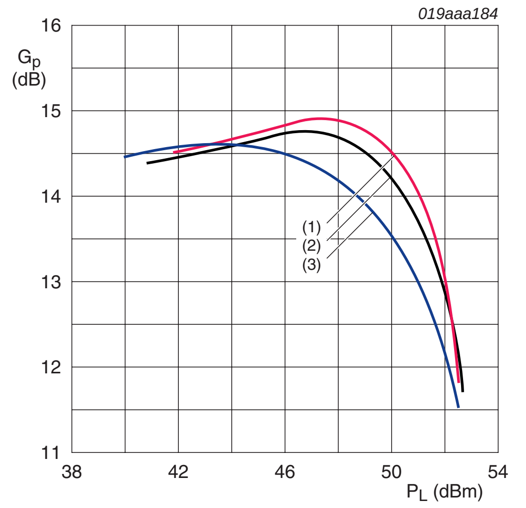


Fig 6. Peak output power as a function of frequency



(1) f = 2500 MHz.

(2) f = 2600 MHz.

(3) f = 2700 MHz.

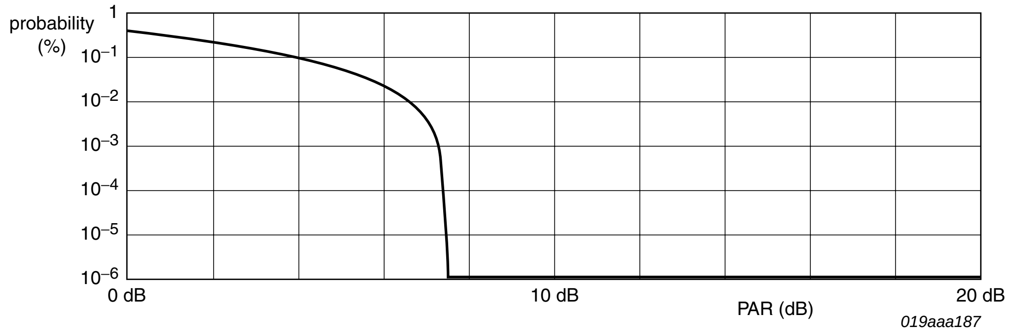
Fig 7. Power gain as a function of output power

4. DPD measurements

4.1 Test signal

The DPD measurements were made using an in-house designed DPD system under the following conditions:

- 2-carrier W-CDMA signal, spacing: 10 MHz, PAR = 7.4 dB at 0.01 % probability (total signal)
- V_{DS} = 28 V, $I_{Dq\ (main)}$ = 500 mA, $V_{GS\ (peak)}$ = 0.4 V



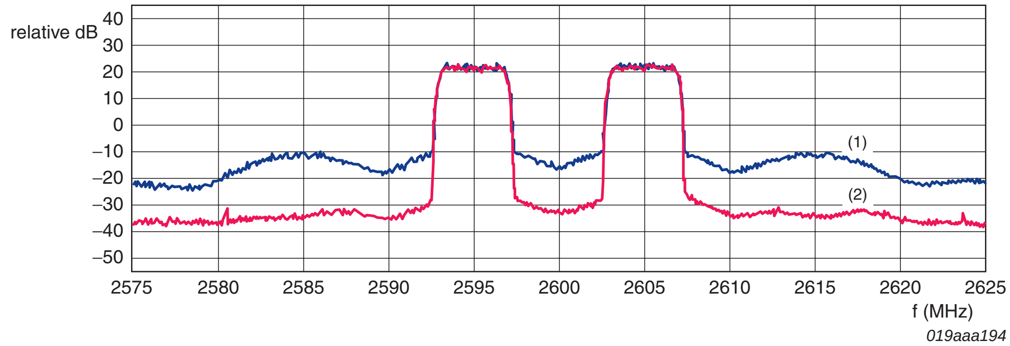
Test signal: 2 carrier W-CDMA, 10 MHz spacing; PAR = 7.4 dB at 0.01% probability.

Fig 8. Test signal CCDF

4.2 2.6 GHz DPD correction

The following DPD measurements were made under the following conditions:

- f_c = 2.6 GHz
- P_L = 45 dBm
- IMD = 15 MHz offset from f_c
- IBW = 3.84 MHz



(1) IMD uncorrected: −33.3 dBc (lower) −33.3 dBc (upper).

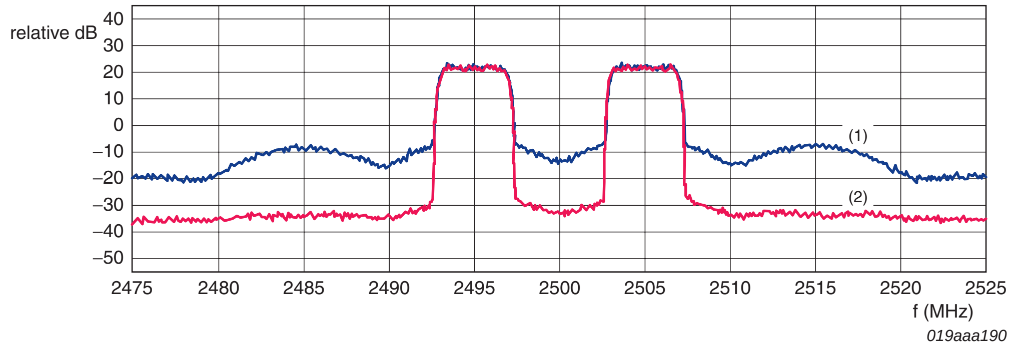
(2) IMD corrected: −55.3 dBc (lower) −55.0 dBc (upper).

Fig 9. DPD measurement; f_c = 2.6 GHz

4.3 2.5 GHz DPD correction

The following DPD measurements were made under the following conditions:

- f_c = 2.5 GHz
- P_L = 45 dBm
- IMD = 15 MHz offset from f_c
- IBW = 3.84 MHz



(1) IMD uncorrected: −30.6 dBc (lower) −29.8 dBc (upper).

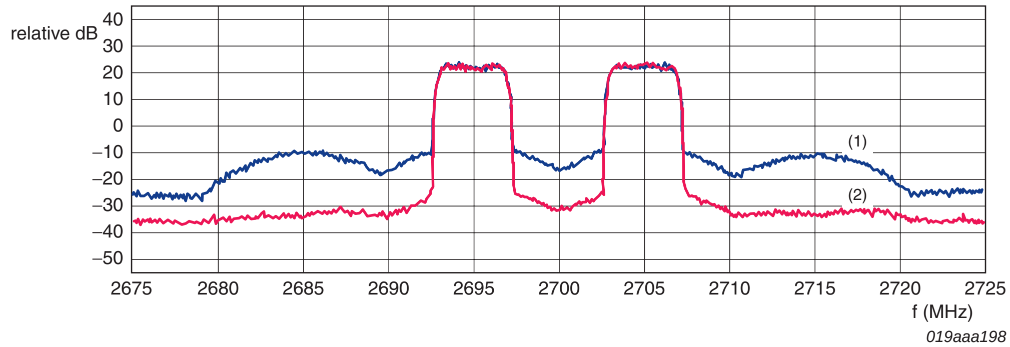
(2) IMD corrected: −55.2 dBc (lower) −54.9 dBc (upper).

Fig 10. DPD measurement, f_c = 2.5 GHz

4.4 2.7 GHz DPD correction

The following DPD measurements were made under the following conditions:

- f_c = 2.7 GHz
- P_L = 45 dBm
- IMD = 15 MHz offset from f_c
- IBW = 3.84 MHz

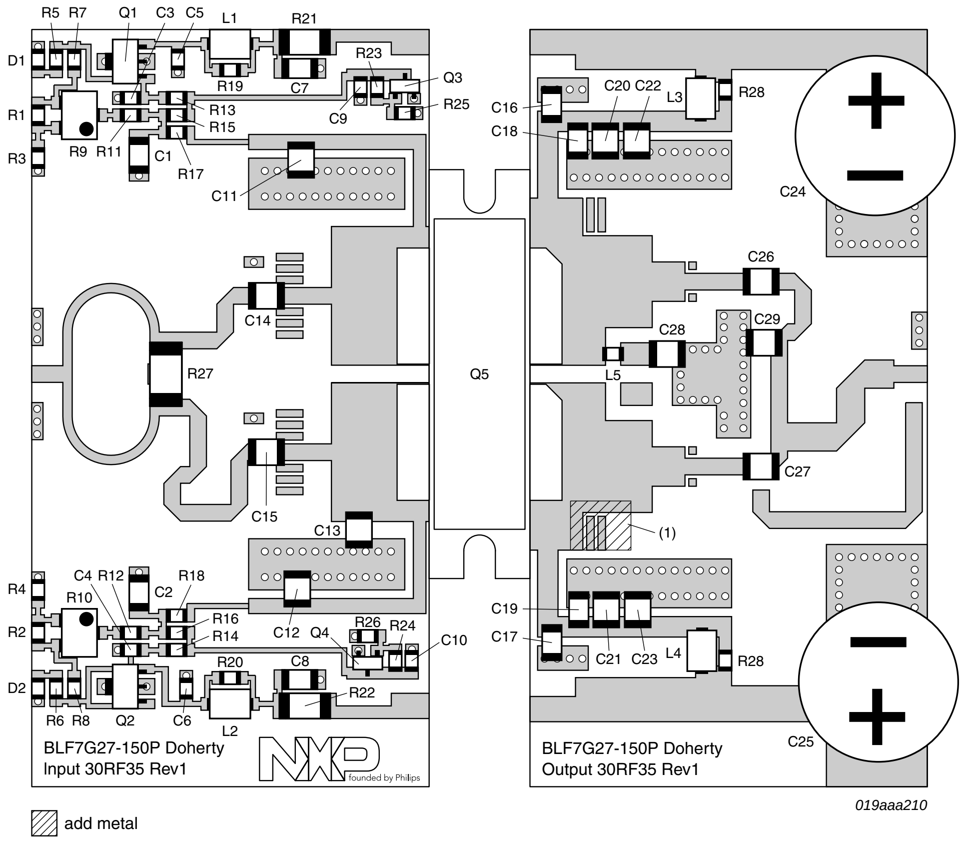


(1) IMD uncorrected: −32.3 dBc (lower) −33.5 dBc (upper).

(2) IMD corrected: −54.8 dBc (lower) −54.5 dBc (upper).

Fig 11. DPD measurement, f_c = 2.7 GHz

5. BLF7G27LS-150P Doherty amplifier board



(1) To ensure RF performance results given in this Application Note, add thin copper to area indicated.

Fig 12. BLF7G27LS-150P Doherty amplifier board component layout

5.1 BLF7G27LS-150P Doherty amplifier board components

Table 1. BLF7G27LS-150P Doherty amplifier board components

Designator	Description	Part identifier	Manufacturer
Input PCB	RF35; ε_r = 3.5; thickness 0.76 mm (0.030")	BLF7G27LS-150P Doherty PA Input-Rev1	Ohio circuits
Output PCB		BLF7G27LS-150P Doherty PA Output-Rev1	Ohio circuits
C1, C2, C7, C8	1 μF ceramic chip capacitor	GRM31MR71H105K88L	MuRata
C3, C4, C5, C6, C9, C10	100 nF ceramic chip capacitor	S0805W104K1HRN-P4	Multicomp
C11, C12	12 pF ceramic chip capacitor	100B	American Technical Ceramics
C13	0.2 pF ceramic chip capacitor	100B	American Technical Ceramics
C14, C15	8.2 pF ceramic chip capacitor	100B	American Technical Ceramics
C16, C17	100 nF ceramic chip capacitor	GRM21BR71H104KA01L	MuRata
C18, C19, C26, C27	12 pF ceramic chip capacitor	100B	American Technical Ceramics
C20, C21, C22, C23, C28	10 μF ceramic chip capacitor	GRM32ER7YA106K88L	MuRata
C24, C25	2200 μF electrolytic capacitor	PCE3474CT-ND	Panasonic
C29	0.4 pF ceramic chip capacitor	100B	American Technical Ceramics
D1, D2	0805 Green SMT LED	APT2012CGCK	KingBright
L1, L2, L3, L4	Ferroxcube bead	2743019447	Fair Rite
L5	3.6 nF inductor		Coilcraft
Q1, Q2	78L08 voltage regulator	NJM#78L08UA-ND	NJR
Q3, Q4	SMT 2N2222 NPN transistor	PMBT2222	NXP Semiconductors
Q5	BLF7G27LS-150P	BLF7G27LS-150P	NXP Semiconductors
R1, R2, R7, R8, R12	432 Ω resistor	CRCW0805432RFKEA	Vishay Dale
R3	75 Ω resistor	CRCW080575R0FKEA	Vishay Dale
R4	0 Ω resistor	CRCW08050R0FKEA	Vishay Dale
R5, R6, R13, R14	1.1 kΩ resistor	CRCW08051K10FKEA	Vishay Dale
R9, R10	200 Ω potentiometer	3214W-1-201E	Bourns
R11	2 kΩ resistor	CRCW08052K00FKTA	Vishay Dale
R15, R16	11 kΩ	CRCW080511K0FKEA	Vishay Dale
R17, R18	5.1 Ω	CRCW08055R1FKEA	Vishay Dale
R19, R20, R28, R29	9.1 Ω resistor	CRCW08059R09FKEA	Vishay Dale
R21, R22	499 Ω/0.25 W resistor	CRCW2010499RFKEF	Vishay Dale
R23, R24	5.1 kΩ resistor	CRCW08055K10FKTA	Vishay Dale
R25, R26	910 Ω resistor	CRCW0805909RFKTA	Vishay Dale
R27	100 Ω/1 W resistor	-	Panasonic

6. Abbreviations

Table 2. Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
DPD	Digital PreDistortion
IBW	Integration BandWidth
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MOSFET	Metal Oxide Silicon Field Effect Transistor
PAR	Peak-to-Average power Ratio
W-CDMA	Wideband Code Division Multiple Access

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